

Nanostructural Investigation on GaAs//Indium Tin Oxide/Si Junctions for III-V-on-Si Hybrid Multijunction Cells

To cite this article: Tomoya Hara *et al* 2020 *ECS Trans.* **98** 125

View the [article online](#) for updates and enhancements.



The banner features a background image of Earth from space. On the left, there are three circular logos: the ECS logo, the Electrochemical Society logo, and the logo for The Korean Electrochemical Society. The central text reads: "Joint International Meeting PRiME 2020 October 4-9, 2020". Below this, a blue bar contains the text "Attendees register at NO COST!". On the right side, there is a large logo for "PRiME™ PACIFIC RIM MEETING ON ELECTROCHEMICAL AND SOLID STATE SCIENCE 2020". At the bottom right, a blue button with white text says "REGISTER NOW ▶".

Nanostructural Investigation on GaAs//Indium Tin Oxide/Si Junctions for III-V-on-Si Hybrid Multijunction Cells

T. Hara^a, J. Liang^a, K. Araki^b, T. Kamioka^b, H. Sodabanlu^c, K. Watanabe^c,
M. Sugiyama^c, and N. Shigekawa^a

^a Osaka City University, Osaka, Japan

^b Toyota Technological Institute, Nagoya, Japan

^c The University of Tokyo, Tokyo, Japan

We investigate nanostructural properties of GaAs//indium tin oxide (ITO)/Si junctions fabricated by surface-activated bonding with emphasis on impacts of thermal process. Both of the Ga 2p_{3/2} and As 2p_{3/2} core-level spectra obtained by hard X-ray photoemission spectroscopy show that the GaAs layers are oxidized by annealing at 400 °C. This finding is consistent with the formation of amorphous-like layers at 400 °C annealed GaAs//ITO interfaces. Concentration depth profiles of O, Ga, and As suggest that the oxidation markedly occurs at GaAs//ITO interfaces annealed at temperatures higher than 200 °C, which is consistent with the dependence of resistance in GaAs//ITO/Si junctions on annealing temperature. These results suggest that annealing brings about the reaction between GaAs and ITO layers and causes the degradation of the electrical properties of GaAs//ITO interfaces. Low-temperature process technologies are essential so as to make a full use of ITO as intermediate layers in III-V-on-Si multijunction cells.

Introduction

III-V-on-Si multijunction (MJ) solar cells are attractive as low-cost and high-efficiency next-generation solar cells (1–3). Given that a high density of dislocations (4) and cracks (5) are reportedly apparent in GaAs layers epitaxially grown on Si substrates due to a large mismatch in the lattice constants and thermal expansion coefficients between GaAs and Si, several bonding technologies such as conventional direct bonding (6), smart stack approach (7) and surface activated bonding (SAB) (8–11) have been applied for fabricating III-V-on-Si MJ cells.

In the SAB process (12), surfaces of substrates to be bonded are irradiated by the fast atom beam (FAB) of Ar. Then the surfaces are activated so that dissimilar materials with different lattice constants and thermal expansion coefficients are directly bonded. It was found by using cross-sectional transmission electron microscopy (XTEM) that amorphous-like intermediate layers were formed at as-bonded Si//Si (13) and GaAs//Si (14) interfaces and the amorphous-like layers were recrystallized by annealing. Hard X-ray photoemission spectroscopy (HAXPES) (15, 16) was applied for examining impacts of annealing on chemical bonds at GaAs//Si interfaces (17). As for the electrical properties, it was found that interface states were introduced to bonding interfaces by Ar

FAB irradiation during the SAB process, which caused depletion in the vicinity of interfaces and an increase in the interface resistance (18).

We proposed the application of indium tin oxide (ITO) intermediate layers so as to reduce the influence of the interface states. We obtained a lower series resistance in InGaP/GaAs//ITO/Si triple-junction cells in comparison with triple-junction cells without ITO layers (19). We observed, however, larger interface resistances for GaAs//ITO/Si junctions when we annealed them at higher temperatures (20). Given that the change in the resistivity of ITO films due to the annealing is not enough to explain the increase of interface resistance, the nano-scale properties of GaAs//ITO interfaces should be examined so as to clarify the mechanism. In this work, we investigate impacts of thermal process on nanoscale structures in GaAs//ITO/Si junctions by HAXPES. We also examine the concentration depth profiles (CDPs) of elements in the vicinity of GaAs//ITO interfaces using X-ray photoelectron spectroscopy (XPS) and Ar⁺ sputter.

Experimental method

We deposited a 100-nm ITO film on a Si (100) substrate. We bonded a GaAs/InGaP epitaxial substrate, which was composed of a 150-nm InGaP etch stopper and an 800-nm GaAs layer grown on a GaAs (100) substrate, to the ITO film using SAB. The substrates were not heated during the bonding process. After annealing at 400 °C for 1 min in N₂ ambient, the GaAs substrate and InGaP etch stopper were eliminated by using selective wet etching. By subsequently etching the GaAs layer, we prepared ~30-nm GaAs//ITO/Si junctions for HAXPES measurements, which were carried out using BL47XU at SPring-8 (21) with a take-off angle of 40°. The X-ray beam used for HAXPES was monochromatized with Si (111) double-crystal and Si (444) channel-cut monochromators, which provides a 7940-eV X-ray with a bandwidth of ~40 meV, a focal spot size of 30 μm (horizontal) by 40 μm (vertical), and a flux of 2.8×10^{11} photons/s. AVG Scienta R4000 hemisphere electron analyzer was used. The binding energy of the HAXPES spectra was calibrated using the Fermi energy of an Au reference. Photoelectron signals due to Ga 2p_{3/2} and As 2p_{3/2} core levels were examined. For XPS measurements we prepared 100-nm ITO//GaAs junctions by bonding ITO films deposited on Si (100) substrates to GaAs (100) substrates, annealing at different temperatures (100, 200, 300, and 400 °C) for 1 min in N₂ ambient, and dissolving the Si substrates using a 30% KOH solution heated to 80 °C. Shimadzu ESCA-3400HSE model in combination with 1.0-keV and 20-mA Ar⁺ sputter was used so as to examine the CDPs of the respective elements.

Results

The Ga 2p_{3/2} core-level spectra of GaAs//ITO interfaces without and with annealing at 400 °C are shown in Fig. 1(a). The background was subtracted using the Shirley method (22). By fitting to the Voigt function, we found that the spectra were dissolved into three peaks. Curves obtained by fitting were in good agreement with the experimental results as is shown in this figure. The extracted binding energies, ~1117.4, ~1118.1, and ~1118.8 eV, were attributed to Ga-As (1117.4 eV), Ga-O in Ga₂O (1118.1 eV) and Ga-O in Ga₂O₃ bonds (1118.8 eV), respectively, by comparing with literatures (23–25). The ratio of Ga-O intensities to Ga-As ones (Ga-O/Ga-As) was estimated to be 0.24 and 2.79 for

interfaces without and with annealing, respectively. The As 2p_{3/2} core-level spectra of GaAs//ITO interfaces are shown in Fig. 1(b). Using the same fitting process for the Ga 2p_{3/2} spectra, the respective As 2p_{3/2} spectra were separated into two peaks with binding energies of ≈ 1323.0 and ≈ 1326.0 eV. Curves obtained by fitting are also shown in the figure. The binding energies were attributed to As-Ga (1323.0 eV) and As-O bonds (1326.0 eV) (23, 24, 26–28), respectively. The As-O/As-Ga ratio was 0.11 and 0.53 for interfaces without and with annealing, respectively. The binding energies and full widths at half maximum of the respective peaks as well as the Ga-O/Ga-As and As-O/As-Ga ratios are summarized in Table I. The intensity ratios observed for GaAs//Si interfaces without and with 400-°C annealing (17) are also shown for comparison. Notably both of the Ga-O/Ga-As and As-O/As-Ga ratios increased for GaAs//ITO interfaces by annealing at 400 °C, while the ratios decreased by annealing GaAs//Si interfaces.

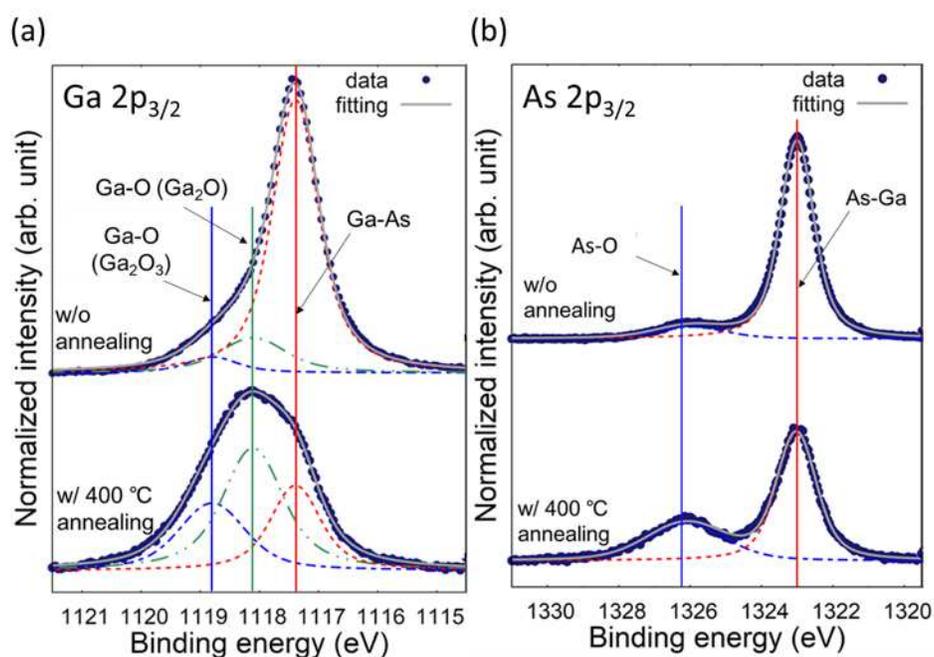


Figure 1. (a) Ga 2p_{3/2} core-level spectra and (b) As 2p_{3/2} core-level spectra of GaAs//ITO interfaces without and with annealing at 400 °C.

Table I. Binding energy and intensity ratio of peaks in Ga 2p_{3/2} and As 2p_{3/2} core-level spectra of GaAs//ITO interfaces. Intensity ratio measured for GaAs//Si junctions (ref. 17) is also shown.

Interfaces (annealing condition)	Binding energy (eV)/FWHM (eV)					Intensity ratio	
	Ga-O (Ga ₂ O ₃)	Ga-O (Ga ₂ O)	Ga-As	As-O	As-Ga	Ga-O/Ga-As	As-O/As-Ga
GaAs//ITO (w/o annealing)	1118.8/1.0	1118.1/1.3	1117.4/0.9	1326.0/2.3	1323.0/1.1	0.24	0.11
GaAs//ITO (400 °C/1 min.)	1118.8/1.3	1118.1/1.2	1117.4/1.0	1326.1/2.6	1323.0/1.3	2.79	0.53
GaAs//Si (w/o annealing)	–					3.94	0.83
GaAs//Si (400 °C/1 min.)	–					0.75	0.09

XTEM images of the GaAs//ITO interfaces without annealing and with 400-°C annealing are shown in Figs. 2(a) and 2(b), respectively. A ≈ 1 -nm thick amorphous-like intermediate layer was observed at the interface with the 400-°C annealing, while such an intermediate layer was not apparent at the interface without annealing.

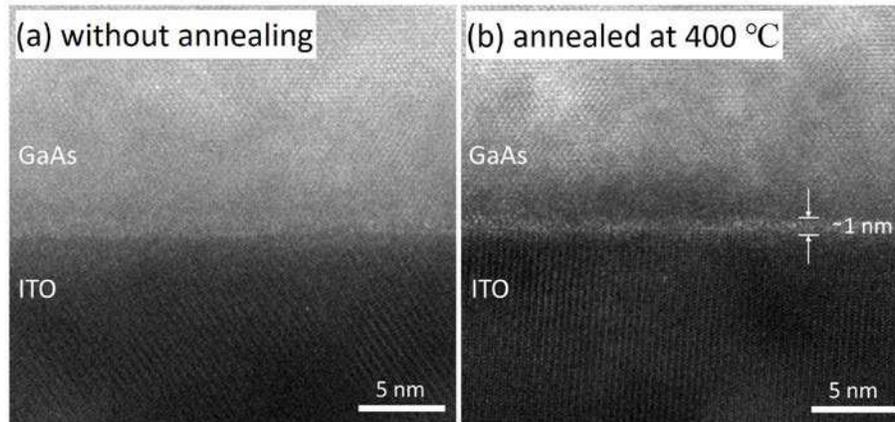


Figure 2. Cross-sectional TEM images of GaAs//ITO interfaces (a) without annealing and (b) annealed at 400 °C.

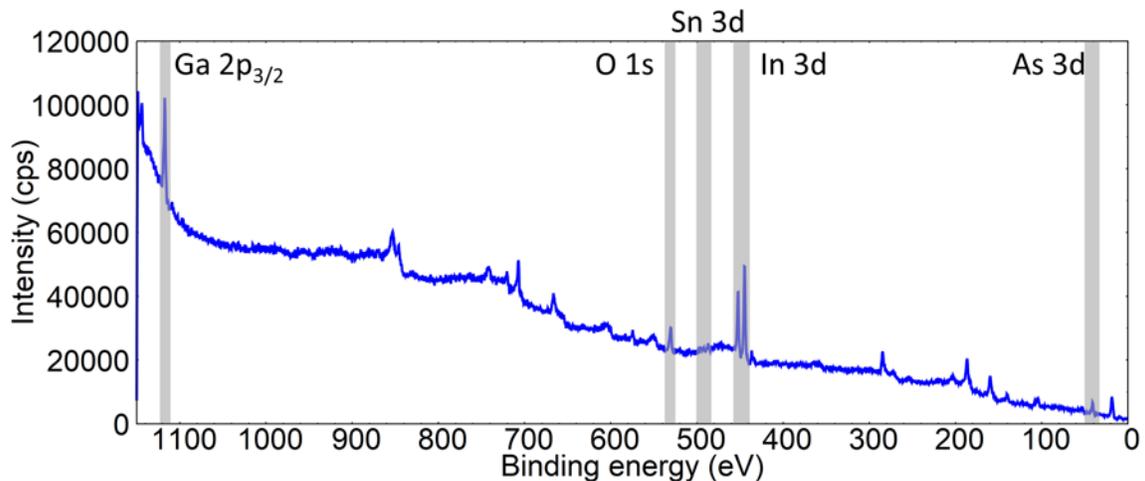


Figure 3. A wide-range XPS spectrum of an ITO//GaAs interface without annealing at a sputter time of 840 s.

Figure 3 shows a wide-range XPS spectrum of ITO//GaAs interfaces obtained at the sputter time t of 840 s. Signals due to In 3d, Sn 3d, O 1s, Ga 2p_{3/2}, and As 3d orbits were apparent. Their contributions were quantified by subtracting a linear background from the obtained signals so that the atomic concentrations of In, Sn, O, Ga, and As were extracted. Their CDPs, or the relationships between the atomic concentrations and t for the respective elements, are shown in Figs. 4(a)-4(e) for ITO//GaAs interfaces without and with annealing at 100, 200, 300, and 400 °C, respectively. CDPs of O, Ga, and As of surfaces of unprocessed GaAs (100) substrates are shown in Fig. 4(f).

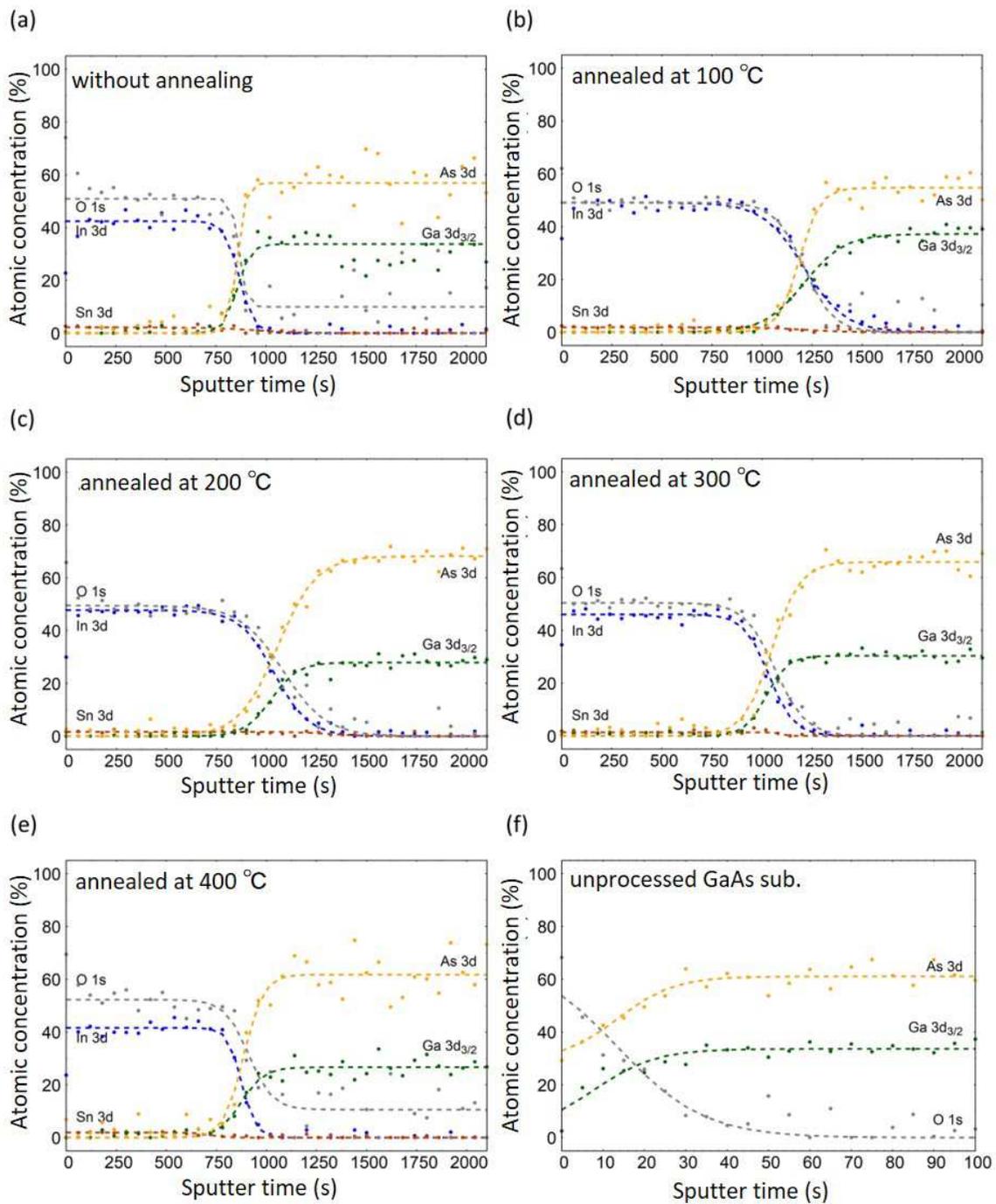


Figure 4. Concentration depth profiles (CDPs) of In, Sn, O, Ga, and As for ITO//GaAs interfaces (a) without annealing and with annealing at (b) 100, (c) 200, (d) 300, and (e) 400 °C, and (f) CDPs for unprocessed surfaces of GaAs (100) substrates.

The experimental CDP data were fit to the Boltzmann sigmoid function, which is given by

$$f(t) = (A_1 - A_2)/(1 + \exp(a(t-t_0))) + A_2 \quad [1]$$

where A_1 , A_2 , a , and t_0 are parameters to fit. The results of fitting are also shown in the respective figures. The estimated t_0 , the time for the halfway between the minimum and maximum for each CDP curve, is summarized in Table II. Results for unprocessed surfaces of GaAs (100) substrates are also shown. We find that $\Delta t_{0,O-Ga}$ ($\equiv t_{0,O} - t_{0,In}$, the difference in t_0 between O and In), $\Delta t_{0,O-Ga}$ ($\equiv t_{0,O} - t_{0,Ga}$), and $\Delta t_{0,O-As}$ ($\equiv t_{0,O} - t_{0,As}$) roughly increase as the annealing temperature increases.

Table II. t_0 and Δt_0 of In, Ga, As, O of GaAs//ITO interfaces and unprocessed surfaces of GaAs (100) substrates.

	t_0 (s)				Δt_0 (s)		
	In	Ga	As	O	O-In	O-Ga	O-As
GaAs//ITO interfaces							
without annealing	867.0	855.9	855.9	867.0	0.0	11.1	11.1
100 °C annealed	1210.4	1210.4	1186.0	1210.4	0.0	0.0	24.4
200 °C annealed	1038.6	1023.1	1056.2	1083.6	45.0	60.5	27.4
300 °C annealed	1035.6	1021.2	1050.3	1065.7	30.1	44.5	15.4
400 °C annealed	876.2	873.3	885.8	910.9	34.7	37.6	25.1
surface of GaAs sub.*	–	11.7	15.2	18.1	–	6.4	2.9

* Time corresponding to halfway of atomic concentrations at $t=0$ and ∞ .

Discussions

The decrease in the Ga-O/Ga-As and As-O/As-Ga ratios observed for annealed GaAs//Si interfaces [Table I] was attributed to the reduction of oxide layers formed during the surface activation process (17). The results of the present work, the increase in Ga-O/Ga-As and As-O/As-Ga ratios due to the annealing, suggest that the reaction between GaAs and ITO occurred and transition layers, which were assumed to be composed of partly-oxidized GaAs, were formed at the interfaces. This view is supported by the result that amorphous-like layers were observed at the 400 °C annealed GaAs//ITO interfaces by XTEM characterization.

We rudely assume that t_0 of CDP curves corresponds to the edge of distribution of the respective elements although the observed curves are likely to be influenced by surface roughness, atomic mixing, or preferential sputtering during the Ar^+ sputter (18). On this assumption, $\Delta t_{0,O-Ga}$, $\Delta t_{0,O-As}$, and $\Delta t_{0,O-In}$ give a measure of the reaction between GaAs and ITO at the bonding interfaces. We estimated the thickness of transition layers with reference to the etching rate of GaAs due to the Ar^+ sputter, which was found to be 0.19 nm/s in a preparatory study. The relationship between the transition layer thickness and t is shown in Fig. 5. The thickness of native oxides on surfaces of GaAs substrates, which was estimated using the same method, is also shown. We find that the transition layer is formed when the junctions are annealed at temperatures higher than 200 °C. The observed behavior is consistent with our previous finding that the electrical resistance of GaAs//ITO junctions drastically increased irrespective of the polarities of GaAs layers when they were annealed at such temperatures. The difference in the thickness of transition layers obtained by analyzing CDPs (≈ 6 nm at 400 °C) and the thickness of

amorphous-like layers in XTEM image (≈ 1 nm) might be due to the parasitic effects caused by the Ar^+ sputter and the uncertainty in etching rate of partly-oxidized GaAs layers. The obtained results imply that III-V-on-Si junctions for hybrid MJ cells should be processed in low-temperature (< 200 °C) environments for fully utilizing ITO as intermediate layers in hybrid MJ cells.

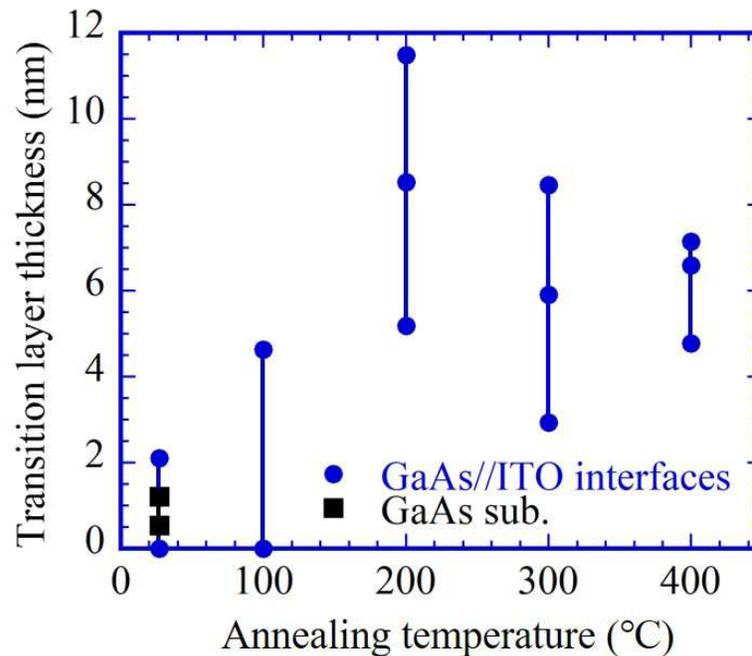


Figure 5. The estimated thickness of transition layers for ITO//GaAs interfaces as function of annealing temperature. The thickness of native oxides on unprocessed GaAs substrates is also shown.

Conclusion

We examined effects of thermal process on nanostructural properties of GaAs//ITO interfaces that were fabricated by using the surface activated bonding technologies. Hard X-ray photoemission spectroscopy analyses indicated that the contribution of chemical bonds to O in the Ga 2p_{3/2} and As 2p_{3/2} core-level spectra was enhanced in the 400 °C annealed junctions, which implied that the GaAs layers were oxidized in the vicinity of GaAs//ITO interfaces. The concentration depth profiles obtained by X-ray photoelectron spectroscopy in combination with Ar^+ sputter suggested that the oxidation of GaAs layers markedly occurred when the annealing temperature was higher than 200 °C, which agreed with the increase of resistance across GaAs//ITO junctions due to the annealing. The results of the present work imply that the low-temperature process is needed so as to apply ITO films for intermediate layers in III-V-on-Si multijunction solar cells.

Acknowledgments

HAXPES measurements were performed at the BL47XU of SPring-8 with the approval of the Japan Synchrotron Radiation Research Institute (JASRI) (Proposal No. 2016A1219, 2017A1005, 2017B1311). The authors are grateful to Prof. K. Ttsuji of Graduate School

of Engineering, Osaka City University for his advice and supports in XPS analyses. This work was supported by the “Research and Development of ultra-high efficiency and low-cost III-V compound semiconductor solar cell modules (High efficiency and low-cost III-V/Si tandem)” project of New Energy and Industrial Technology Development Organization (NEDO). A part of this work was supported by Kyoto University Nano Technology Hub in “Nanotechnology Platform Project” sponsored by the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan.

References

1. S. R. Kurtz, P. Faine, and J. M. Olsom, *J. Appl. Phys.*, **68**, 1980 (1990).
2. T. Soga, T. Kato, K. Baskar, C. L. Shao, T. Jimbo, and M. Umeno, *J. Crystal Growth*, **170**, 447 (1997).
3. M. Umeno, T. Soga, K. Baskar, and T. Jimbo, *Sol. Energy Mater. Sol. Cells*, **50**, 203 (1998).
4. M. Yamaguchi, M. Tachikawa, Y. Itoh, M. Sugo, and S. Kondo, *J. Appl. Phys.*, **68**, 4518 (1990).
5. V. K. Yang, M. Groenert, C. W. Leitz, A. J. Pitera, M. T. Currie, and E. A. Fitzgerald, *J. Appl. Phys.*, **93**, 3859 (2003).
6. K. Tanabe, K. Watanabe, and Y. Arakawa, *Scientific Reports*, **2**, 349 (2012).
7. H. Mizuno, K. Makita, T. Tayashi, T. Mochizuki, T. Sugaya, and H. Takato, *Appl. Phys. Express*, **10**, 072301 (2017).
8. S. Essig, J. Benick, M. Schachtner, A. Wekkeli, M. Hermle, and F. Dimroth, *IEEE J. Photovolt.*, **5**, 977 (2015).
9. N. Shigekawa, J. Liang, R. Otsuka, T. Agui, H. Juso, and T. Takamoto, *Jpn. J. Appl. Phys.*, **54**, 08KE03 (2015).
10. R. Cariou, J. Benick, P. Beutel, N. Razek, C. Flötgen, M. Hermle, D. Lackner, S. W. Glunz, A. W. Bett, M. Wimplinger, and F. Dimroth, *IEEE J. Photovolt.*, **7**, 367 (2017).
11. S. Essig, C. Allebé, T. Remo, J. F. Geisz, M. A. Steiner, K. Horowitz, L. Barraud, J. S. Ward, M. Schnabel, A. Descoeurdes, D. L. Young, M. Woodhouse, M. Despeisse, C. Ballif, and A. Tamboli, *Nat. Ene.*, **2**, 17144 (2017).
12. H. Takagi, K. Kikuchi, R. Maeda, T. R. Chung, and T. Suga, *Appl. Phys. Lett.*, **68**, 2222 (1996).
13. H. Takagi, R. Maeda, N. Hosoda, and T. Suga, *Jpn. J. Appl. Phys.*, **38**, 1589 (1999).
14. Y. Ohno, J. Liang, N. Shigekawa, H. Yoshida, S. Takeda, R. Miyagawa, Y. Shimizu, and Y. Nagai, *Appl. Surf. Sci.*, **525**, 144610 (2020).
15. N. Benito, R. E. Galindo, J. R. Zuazo, G. R. Castro, and C. Palacio, *J. Phys. D: Appl. Phys.*, **46**, 065310 (2013).
16. S. Toyoda and M. Oshima, *J. Appl. Phys.*, **120**, 085306 (2016).
17. S. Yamajo, S. Yoon, J. Liang, H. Sodabanlu, K. Watanabe, M. Sugiyama, A. Yasui, E. Ikenaga, and N. Shigekawa, *Appl. Surf. Sci.*, **473**, 627 (2019).
18. M. Morimoto, J. Liang, S. Nishida, and N. Shigekawa, *Jpn. J. Appl. Phys.*, **54**, 030212 (2015).
19. N. Shigekawa, T. Hara, T. Ogawa, J. Liang, T. Kamioka, K. Araki, and M. Yamaguchi, *IEEE J. Photovolt.*, **8**, 879 (2018).

20. T. Hara, T. Ogawa, J. Liang, K. Araki, T. Kamioka, and N. Shigekawa, *Jpn. J. Appl. Phys.*, **57**, 08RD05 (2018).
21. E. Ikenaga, A. Yasui, N. Kawamura, M. Mizumaki, S. Tsutsui, and K. Mimura, *Synchrotron Radiation News*, **31**, 10 (2018).
22. D. A. Shirley, *Phys. Rev. B*, **5**, 4709 (1972).
23. G. Cossu, G. M. Ingo, G. Mattogno, G. Padeletti, and G. M. Proietti, *Appl. Surf. Sci.*, **56-58**, 81 (1992).
24. M. Paul, A. Müller, A. Ruff, B. Schmid, G. Berner, M. Mertin, M. Sing, and R. Claessen, *Phys. Rev. B*, **79**, 233101 (2009).
25. C. L. Hinkle, M. Milojevic, B. Brennan, A. M. Sonnet, F. S. Aguirre-Tostado, G. J. Hughes, E. M. Vogel, and R. M. Wallace, *Appl. Phys. Lett.*, **94**, 162101 (2009).
26. J. A. Taylor, *J. Vac. Sci. Technol.*, **20**, 751 (1982).
27. M. K. Bahl, R. O. Woodall, R. L. Watson, and K. J. Irgolic, *J. Chem. Phys.*, **64**, 1210 (1976).
28. J. Massies and J. P. Contour, *J. Appl. Phys.*, **58**, 806 (1985).